REMARKS

Formal Drawings have been submitted and are attached. Applicants respectfully request that the examiner withdraw the objections to the drawings.

Claims 22-27 have been added. Support for claim 22 may be found throughout the specification and drawings, including paragraph 11. Support for claim 23-27 may be found in at least FIGS. 2A-2D and the associated description. No new matter has been entered.

Claim rejections under 35 U.S.C. 112

The examiner had rejected claim 13 under 35 U.S.C. 112, second paragraph. , particularly the phrase "in a tone reversed form that used for patterning and etching the dielectric". Applicants have amended the claim language to clarify the meaning of the words used. As known to those of skill in the art, photomasks such as for example patterned glass photomasks are used to transfer the pattern appearing on the glass photomask to a resist layer on the substrate, a thin layer of polymeric material coated on the substrate. The resist layer may be either a positive resist or a negative resist. Light is directed through he chrome on glass mask to expose the photoresist. With a positive photoresist, i.e., a photoresist having a positive tone, exposed areas become more soluble in a subsequently applied developing solution than the unexposed areas. With a negative resist, the exposed areas become less soluble. It is these differences in solubility that permit the pattern transfer into the resist image. In the amended claim, it is these different types of photoresist which are referred to by the recited term "tone". Applicants therefore respectfully request that the Examiner withdraw the objection.

Claim rejections under 35 U.S.C. 103

The examiner rejected claim 12 under 35 U.S.C. 103 as unpatentable over McTerr and Robinson. Applicants respectfully traverse the rejections.

McTerr is generally directed to the migration of interconnects from Cu to Al and addresses diffusion barriers. Specifically, McTerr relates to improved methods for filling openings in silicon substrates with copper (17: 14-22). McTerr describes the conventional formation of copper interconnects by damascene methods, that is, by etching a dielectric layer to form a channel and filling the channel with copper. As is known to those of skill in the art, copper diffusion barrier layers typically comprise Ta or TaN and are usually deposited in trenches formed in insulating layers prior to depositing copper. This barrier layer is necessary to prevent the copper from poisoning the dielectric. As McTerr notes, these barrier layers are not stable at the high temperatures necessary for reflow, for example, as required in high aspect ratio openings, according to McTerr.

In rejecting the claims, the examiner has based the rejection on various figures (e.g., FIGS. 1-6, and 14) in McTerr, and typically portions of the detailed specification referring to those figures. These figures generally describe alternative embodiments and thus they cannot in most cases be combined to suggest the stages in formation. FIG. 1 describes a method of using a $Ti_xAl_yN_x$ barrier layer prior to filling the damascene trench with copper. FIG. 2 describes an alternative method of filling the trench by first using a copper diffusion barrier layer (such as TaN or $Ti_xAl_yN_x$) followed by an aluminum wetting layer and then the copper fill step. FIG. 3 describes a method similar to that of FIG. 2, but after depositing the copper, the structure is annealed and caused to reflow. It should be noted that typically barrier layers are very thin. McTerr is consistent with this view, indicating that the barrier layers of the figures have a maximum size of 500A for FIG.1 and 2000A for FIG.2. It should further be noted that one of skill in the relevant art would not reasonably interpret the barrier layer as either an aluminum layer or a copper layer. That is, the copper diffusion barrier layer contains no copper and the aluminum barrier layer in one aspect contains a maximum of 15% aluminum (17:40-45).

FIGS. 4-6 show cross sections of contact level dual damascene structures. These are typically referred to as contract level since a conducting portion of the dual damascene structure forms an electrical contact with a contact to diffusion area of the silicon portion of the wafer, such as the silicided region 11 shown. FIG. 4 shows the trench and via of the dual damascene

structure first filled with a refractory metal (100 to 800A) followed by a $Ti_xAl_yN_x$ barrier layer. And then filled with copper. FIG. 5 shows an alternative with the dual damascene opening subjected to the depositing of a refractory metal layer, a copper diffusion barrier layer 4, and an aluminum wetting layer 5 prior to the filling with copper. FIG. 6 is similar and shows the trench and via overlaid with a refractory metal layer, a copper diffusion barrier layer 4, an aluminum wetting layer 5 prior to the filling with copper and the anneal and copper reflow steps.

FIG. 14 shows a via level aluminum copper dual damascene interconnect. That is, as shown, the dual damascene structure is formed above an aluminum line 16 formed in the second insulating layer 9. This line is shown formed above conductive metal plug 8, which is formed in first insulating layer 7, the insulating layer 7 being formed on the silicon substrate 10. Since no barrier layer is shown for the conductive metal plug 8, this would not be interpreted by one of skill to comprise either cu or al.

On page 4 of the office action the examiner indicates that McTerr teaches depositing an aluminum layer on at least a portion of the top polished surface of the dielectric and at least a portion of the top polished surface of the copper of the first planarized surface is taught or suggested. McTerr does not teach this. It isn't clear from the paragraph whether the Examiner is referring to FIGS. 3, 6 or FIG. 14 to support his position. Applicants assume from the context that the examiner intends to rely on McTerr FIG. 14 and col.22, lines 45-50. From the drawing, the only planarized surface having a top polished surface of copper is the surface line at the top of insulator 14. There is no aluminum layer disclosed as deposited on this planarized surface. Since this Figure is described as a via level dual damascene, it would be understood from the drawing and description by one of skill in the art to involve planarization only after the copper fill step. The conductive plug 8, shown as connected to the silicon substrate 10, is not specifically defined with respect to this drawing but in a similar drawing (FIG. 7) is noted to be made from tungsten in one example. One skilled in the art would not recognize the drawing to intend the plug to be made from copper , for at least the reason that the necessary copper barrier layers are not shown deposited into the hole before the plug is filled. Moreover, the pug does not comprise an interconnect line but instead connect different interconnect lines to a diffusion area.

Alternatively, There is no planarized surface of copper and dielectric suggested in any of FIGS. 1-3. In Fig. 6, although there is a planarized surface of insulator 9 and copper 3 at the topmost portion of insulator 9, there is no teaching of depositing an aluminum layer on the planarized surface as required by claim 12. Therefore, for at least the various reasons listed above, McTerr fails to teach or suggest al of the elements of claim 1.

The examiner acknowledge that McTerr doesn't teach an etching step, but states that Robinson does so at col. 8, lines 13-18, and further state that it would be obvious to one of ordinary skill in the art to include Robinson's etching step as part of patterning step in McTerr's process steps to form a patterned aluminum layer that acts as a catalyst in preventing native oxide formation from the titanium containing material allowing the deposition of copper layer with fewer impurities..." Applicants respectfully disagree. There would be no motivation to combine McTerr with Robinson and even if they were combined, they still fail to teach all elements of claim 1. Robinson generally relates to a method for depositing copper on a titanium containing surface of a substrate (abstract). Aluminum is described and shown to be patterned to form a catalyst layer. For example, FIG. 3A shows an aluminum layer formed on a titanium layer and later patterned to exposed the via and to allow copper to fill the via to form a plug (12: 50-67). The aluminum layer 26 is then removed (13: 20-30). Thus, even though Robinson may teach patterning of the aluminum, the aluminum layer does not form part of the interconnect. That is, even combining the references, they still fail to teach the dual layer interconnect of claim 1 wherein the upper aluminum layer forms the upper conductive metal portion of the interconnect.

Applicants note that the examiner appears to be basing his rejection at least in part on the assumption that an underlying aluminum layer is equivalent to an overlying aluminum layer. This is not the case. For example, providing an upper aluminum layer provides advantages that can't be achieved in the same way by using copper on top. For example, bond pads, such as formed in bond pad layers, require aluminum since the packaging processes have not matured sufficiently to bond directly to copper. Moreover, placing copper layers on top of aluminum

would require a capping layer or other barrier layer to prevent copper diffusion into the overlying dielectric.

In view of the foregoing discussion, the rejections of claim 12 over both McTerr and Robinson are believed overcome. The rejections of claims 13-20 and 22 are believed overcome for at least their dependencies from claim 12. Claim 23 is submitted to be allowable for at least the same reasons discussed above. Moreover, none of the references, alone or in combination, teach or suggest depositing or patterning and etching the pad metal layer to define the upper portion of the interconnect as recited in claim 1. cancelled - should be claim 12

The Applicant respectfully acknowledges the indications that claim 21 contains allowable subject matter. However, in view of the foregoing discussion, claim 21 is believed to be allowable in its present condition without amendment.

Conclusion

Accordingly, it is submitted that all issues in the Office Action have been addressed, and withdrawal of the rejections is respectfully requested. Applicants believe that this application is in condition for allowance, and respectfully request a prompt passage to issuance. If the Examiner believes that a telephone conference would expedite the prosecution of this application, he is invited to contact the Applicants' undersigned attorney at the telephone number set out below.

Respectfully submitted,
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